Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Please amend the claims as follows:

1. (Currently Amended) An apparatus comprising:

a memory;

a plurality of processors coupled to the memory; and

a controller coupled to the memory and the plurality of processors, the controller to execute a debug process that:

attaches at least one breakpoint bit field comprising a single bit directly to one or more instructions of the plurality of processors, [[the]] each breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of an instruction of the one or more instructions ~~that the~~ to which breakpoint bit field is attached without having to perform an address comparison;

manipulates at least three debug register bit fields of at least one processor control status register, the at least three register bit fields comprising a run field, a single step field, and a debug enable field that each comprise a single bit; and

accesses an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM (LDTI) instruction and a Load from Instruction RAM (LDFI) instruction.

2. (Previously Presented) The apparatus of claim 1, wherein said at least one breakpoint bit field allows a breakpoint to be one of set and not set for each of said one or more instructions.

3.-4. (Canceled)

5. (Previously Presented) The apparatus of claim 1, wherein said single step field allows a set of instructions to each be single-stepped through one cycle at a time.

6. (Previously Presented) The apparatus of claim 1, wherein said debug enable field one of enables and disables a debug mode.

7. (Previously Presented) The apparatus of claim 1, wherein the LDTI instruction loads content of a register in a processor of the plurality of processors into an instruction memory coupled to the processor via a bus.

8. (Previously Presented) The apparatus of claim 7, wherein the LDFI instruction loads the content of the instruction memory into the register coupled to the processor.

9. (Canceled)

10-17. (Canceled)

18. (Currently Amended) An apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising:

adding at least one breakpoint bit field comprising a single bit directly to each of a plurality of instructions to execute on a plurality of processors, [[the]] each breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of an instruction of the one or more instructions ~~that the~~ to which breakpoint bit field is attached without having to perform an address comparison;

manipulating at least three debug register bit fields of at least one processor control status register, the at least three register bit fields comprising a run field, a single step field, and a debug enable field, each comprising a single bit; and

accessing an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM (LDTI) instruction and a Load from Instruction RAM (LDFI) instruction.

19. (Currently Amended) The apparatus of claim 18, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of one of said breakpoint bit fields, and

setting a breakpoint for an instruction if it is determined that said state of said ~~at least one~~ breakpoint bit field is set.

20. (Canceled)

21. (Previously Presented) The apparatus of claim 19, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of a run field bit,

running a set of instructions if said state of said run field bit is set, and

stopping a set of instructions if said state of said run field bit is not set.

22. (Previously Presented) The apparatus of claim 21, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of a single step bit, and

single-stepping through a set of instructions for a cycle if said state of said single-step bit is set.

23. (Previously Presented) The apparatus of claim 18, wherein the LDTI instruction loads content of at least one register into an instruction memory, and wherein the LDFI instruction loads content of said instruction memory into the at least one register.

24. (Currently Amended) A method comprising:

adding at least one breakpoint bit field comprising a single bit directly to each of a plurality of instructions to execute on a plurality of processors, [[the]] each breakpoint bit field to enable a user to set a breakpoint based on an address of an instruction of the one or more instructions ~~that the~~ to which breakpoint bit field is attached without having to perform an address comparison;

manipulating at least three breakpoint register bit fields of at least one processor control status register, the at least three register bit fields comprising a run field, a single step field, and a debug enable field, each comprising a single bit; and;

accessing an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM (LDTI) instruction and a Load from Instruction RAM (LDFI) instruction;

wherein the at least one breakpoint bit field is an additional field directly added to each processor instruction.

25. (Previously Presented) The method of claim 24, further comprising:

determining a state of a breakpoint bit, and

setting a breakpoint for an instruction if it is determined that said state of said breakpoint bit is set.

26. (Original) The method of claim 24, further comprising:

running a debug process on a host device, and

entering debug commands through a graphical user interface.

27. (Canceled)

28. (Previously Presented) The method of claim 24, further comprising:

determining a state of a single-step bit, and

entering commands for single-stepping through a set of instructions for a cycle if said state of said single-step bit is set.

29. (Previously Presented) The method of claim 24, wherein the LDTI instruction loads content of at least one register into an instruction memory, and wherein the LDFI instruction loads content of said instruction memory into the at least one register.